1. A method comprising:

implementing read accesses to the same portion of a memory line in the same cycle.

2. The method of claim 1 including determining whether two read accesses are to the same portion of a memory line by determining whether the read accesses are to the same subline.

3. The method of claim 1 including using a modified Harvard architecture.

4. The method of claim 2 including providing a first portion of the subline on a first bus and a second portion of the subline on a second bus.

5. The method of claim 2 including determining that the read accesses are to the same half of a subline and providing that same half on two different output lines.

6. The method of claim 1 wherein determining includes comparing the addresses of two read accesses to determine whether those read accesses access the same subline.

7. The method of claim 6 including generating a read signal if those read accesses access the same subline.

8. The method of claim 7 including determining whether a 64 bit read has been enabled and, if so, accessing two different portions of the same subline in the same read cycle.

9. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

determine whether two read accesses are to the same portion of a memory line; and

if so, implement the read accesses from the portion in the same cycle.

10. The article of claim 9 further storing instructions that enable the processor-based system to determine whether the read accesses are to the same subline.

11. The article of claim 10 further storing instructions that enable a processor-based system to provide a first portion of the subline on a first bus and a second portion of the subline on a second bus.

12. The article of claim 10 further storing instructions that enable the processor-based system to determine that the read accesses are to the same half of a subline and provide that same half on two different output lines.

13. The article of claim 9 further storing instructions that enable the processor-based system to compare addresses to determine whether the read accesses access the same subline.

14. The article of claim 13 further storing instructions that enable the processor-based system to determine whether a 64 bit read has been enabled and, if so, access two different portions of the same subline in the same read cycle.

15. A processor comprising:

a data memory; and

a controller to access said data memory, said controller to implement read accesses to the same portion of a memory line in the same cycle.

16. The processor of claim 15 wherein said controller determines whether the read accesses are to the same subline.

17. The processor of claim 15 wherein said processor uses a modified Harvard architecture.

18. The processor of claim 16 wherein said controller to provide a first portion of the subline on a first bus and a second portion of the subline on a second bus.

19. The processor of claim 16 wherein said controller to determine that the read accesses are to the same half of a subline and provide that same half on two different output lines.

20. The processor of claim 15 wherein said controller to compare the addresses of two read accesses to determine whether said read accesses access the same subline.

21. The processor of claim 20 wherein said controller determines whether a 64 bit read has been enabled and, if so, accesses two different portions of the same subline in the same read cycle.

22. The processor of claim 20 wherein said controller includes a comparator coupled to an AND gate in turn coupled to said data memory.

23. A system comprising:

a digital signal processor;

a general purpose processor;

a bus coupled to said digital signal processor and said general purpose processor; and

said digital signal processor including a data memory and a controller to access the data memory, said controller to determine whether two read accesses are to the same portion of a memory line and, if so, implement the read accesses from the same portion in the same cycle.

24. The system of claim 23 wherein said controller determines whether the read accesses are to the same subline.

25. The system of claim 24 wherein said digital signal processor uses a modified Harvard architecture.

26. The system of claim 24 wherein said controller to provide a first portion of said subline on a first bus and a second portion of said subline on a second bus.

27. The system of claim 24 wherein said controller to determine that the read accesses are to the same half subline and provide that same half on two different output lines.

28. The system of claim 24 wherein said controller to compare the addresses of two read accesses to determine whether said read accesses access the same subline.